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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,592	07/25/2003	Takeshi Matsunaga	240900US2S	9746

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EXAMINER	
ORTIZ, EDGARDO	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 01/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/626,592	MATSUNAGA ET AL.	
	Examiner	Art Unit	
	Edgardo Ortiz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 11-13* is/are rejected.

7)☒ Claim(s) *9 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/25/03*. 6/21/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Species I (Figure I) in the response filed October 7, 2004 is acknowledged. Applicant's arguments regarding that a search and examination can be made without a serious burden on the Examiner, are deemed persuasive and thus all claims (1-13) will be examined and considered as follows.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Moise et al. (U.S. Patent No. 6,734,477). With regard to Claim 1, Moise discloses a semiconductor device having a capacitor formed in a multilayer wiring structure, the semiconductor device comprising:

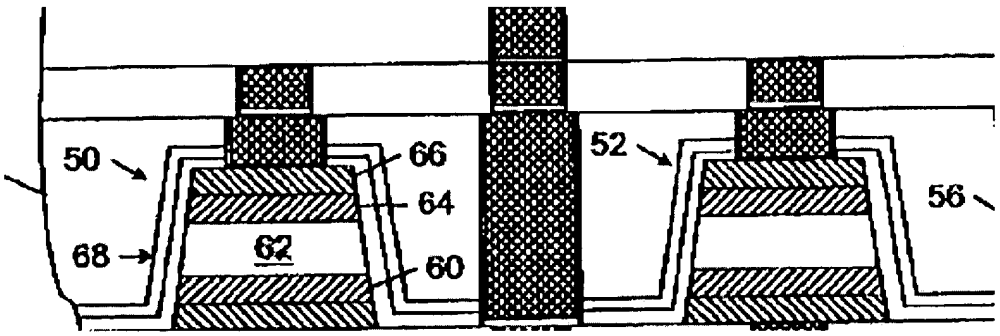
a multilayer wiring structure (figure 1) including a plurality of wirings layers (12, 14, 16, 18, 22) formed on a substrate (26);

a capacitor (50 or 52) arranged in a predetermined wiring layer (16) in the multilayer wiring structure and having a lower electrode (60), a dielectric film (62), and an upper electrode (64);

a first via formed in the predetermined wiring layer (16) and connected (figure 1); to a top surface of the upper electrode (64) of the capacitor (50 or 52); and

a second via formed in an overlying wiring layer (18) stacked on the predetermined wiring layer (16), the second via being formed on the first via (figure 2).

With regard to Claim 2, Moise discloses a first via that is formed to have a larger cross section than that of the second via (figure 1).



With regard to Claim 3, Moise discloses a predetermined wiring layer (16) having a third via formed on the lower electrode (60) and a wiring connected to the third via (column 4, lines 3-7) and buried in a surface of the predetermined wiring layer (figure 1).

With regard to Claim 4, Moise discloses a predetermined wiring layer (16) having a third via formed on the lower electrode (60) and a wiring connected to the third via (column 4, lines 3-7) and buried in a surface of the predetermined wiring layer (figure 1).

With regard to Claim 7, Moise discloses an overlying wiring layer (18) having a wiring connected to the top of the second via and buried in a surface of the overlying wiring layer (figure 1).

With regard to Claim 8, Moise discloses an overlying wiring layer (18) having a wiring connected to the top of the second via and buried in a surface of the overlying wiring layer (figure 1).

With regard to Claim 11, Moise discloses a lower electrode (60) of the capacitor (50 or 52) that is connected to a wiring buried in a surface of an underlying wiring layer (14) formed under the predetermined wiring layer (16) in which the capacitor is formed (figure 1).

With regard to Claim 12, Moise discloses a lower electrode (60) of the capacitor (50 or 52) that is connected to a wiring buried in a surface of an underlying wiring layer (14) formed under the predetermined wiring layer (16) in which the capacitor is formed (figure 1).

With regard to Claim 13, Moise discloses a semiconductor device having a capacitor formed in a multilayer wiring structure, the semiconductor device comprising:

at least one impurity diffusion layer (34 or 36) formed in a first area (figure 1) of a semiconductor substrate (26);

a plurality of wirings layers (12, 14, 16, 18, 22) stacked (figure 1) on the semiconductor substrate (26) and including a first wiring layer (14) having a contact (30) connected to the impurity diffusion (34 or 36) and a first wiring buried so as to connect to the contact (figure 1);

a capacitor formed in a predetermined (16) one of the plurality of wiring layers which predetermined wiring layer is formed on a second area different from the first area of the semiconductor substrate (figure 1), the capacitor having a stacked structure of a lower electrode (60), a dielectric film (62), and an upper electrode (64);

an upper wiring layer (18) having an interlayer insulating film (figure 1) stacked on the predetermined wiring layer (16), a second via formed in the interlayer insulating film, connected to the first via, and a second wiring connected to the second via and buried (figure 1) in a surface portion of the upper wiring layer (18).

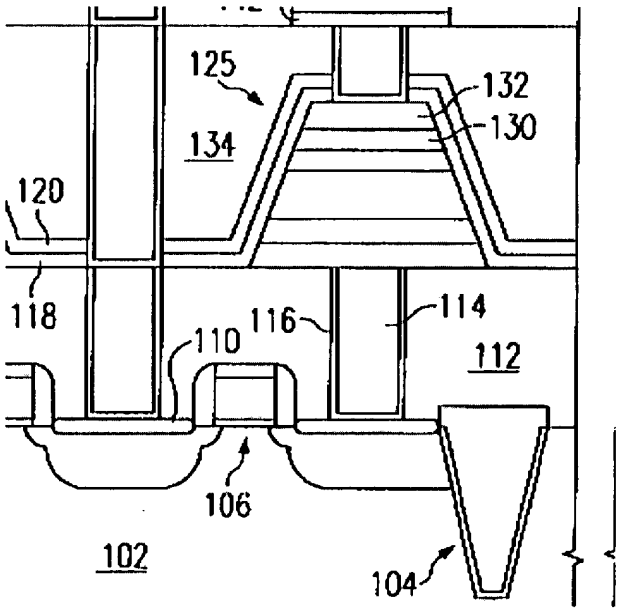
Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moise et al. (U.S. Patent No. 6,734,477) in view of Moise et al. (U.S. Patent No. 6,534,809). With regard to Claims 5-6, Moise ('477) discloses a predetermined wiring layer (16) having a third via formed on the lower electrode (60), a wiring connected to the third via (column 4, lines 3-7) and a metal-diffusion stopper film (column 4, lines 38-42) on a surface of the predetermined wiring layer.

Moise ('477) fails to disclose the claimed wiring comprising copper. However, Moise ('809) discloses (figure 1) a semiconductor device including a capacitor structure (125) having a bottom electrode (124) and a via having a wiring (114) connected to the via, wherein the wiring comprises copper (column 7, lines 42-46).



Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Moise ('477) to include the claimed wiring comprising copper, as suggested by Moise ('809), in order to form contacts to the substrate and gate structures (column 7, lines 39-42) and filled with a material (copper) known in the semiconductor art for its good conductivity.

Allowable Subject Matter

4. Claims 9-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The cited prior art fails to disclose, teach or suggest, at least on claim 9, a semiconductor device including "*a fourth via formed connected to a top of the third via and formed to be thinner than the third via is provided in the overlying wired layer; and the second and fourth vias are connected to the first and second wirings, respectively, buried in a surface of the overlying wiring layer.*"

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edgardo Ortiz whose telephone number is 571-272-1735. The examiner can normally be reached on Monday-Friday (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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